bdiGDB for BDI3000 MPC85xx/P10xx/P2020

Release Note

Config. program ■ V1.01
Firmware for BDI3000 ■ V1.09

Date: June 20, 2008

Enhancements

• Enhanced Telnet „go“ and „halt“ command for MPC8572 dual-core processor.

Error Correction

• Error in e500 GDB register packet format corrected.

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bdiGDB for BDI3000 MPC85xx/P10xx/P2020

Release Note

Config. program ■ V1.02
Firmware for BDI3000 ■ V1.10

Date: Febr. 13, 2009

Enhancements

- Support for MPC8536 added
- New MT Telnet command for a simple bus/memory test added.

Error Correction

- Error when single-stepping in JTAG mode corrected.

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bdiGDB for BDI3000 MPC85xx/P10xx/P2020

Release Note

Config. program ☐ V1.02
Firmware for BDI3000 ■ V1.11

Date: June 24, 2009

Enhancements

- Support for MPC8569 added
- Support for P2020 added

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bdiGDB for BDI3000 MPC85xx/P10xx/P2020

Release Note

Config. program ☐ V1.02
Firmware for BDI3000 ■ V1.12

Date: Febr. 12, 2010

Enhancements

- Support for Boot Page translation added, define „MMU XLAT 0xfffff000“.
- Support for P2020 Rev.2 (new PVR) added.
- Download speed via GDB improved.
- Maximal number of software breakpoints increased to 64.
- Support for GDB p - packet (single register read) added.

Error Correction

- Display all 512 TLB0 entries for e500v2.

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bdiGDB for BDI3000 MPC85xx/P10xx/P2020

Release Note

Config. program ☐ V1.02
Firmware for BDI3000 ■ V1.13

Date: June 25, 2010

Enhancements

- Support for P1020 added
- Some GDB protocol improvements.

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bdiGDB for BDI3000 MPC85xx/P10xx/P2020

Release Note

Config. program ■ V1.03
Firmware for BDI3000 ■ V1.14

Date: June 10, 2011

Enhancements

- Special reset sequence required for P1010/14 added.
- For some devices, overriding the Boot ROM Location is supported via the ROMLOC option.
- GDB hardware watch reporting enhanced by using the T05watch response packet.

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bdiGDB for BDI3000 MPC85xx/P10xx/P2020

Release Note

Config. program ☐ V1.03
Firmware for BDI3000 ■ V1.15

Date: Sept. 9, 2011

Enhancements

• Accept new e500v2 PVR numbers.

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bdiGDB for BDI3000 MPC85xx/P10xx/P2020

Release Note

Config. program ■ V1.05
Firmware for BDI3000 ■ V1.16

Date: May 18, 2012

Enhancements

- Optimized reset sequence for P1010/14.
- Time-out time when waiting for reset released by the target has been increased to 1 second.
- New reset mode KEEP added. KEEP asserts HRESET during the whole target power-up cycle. This was the default mode for older firmware but some boards could not be connected this way.
- The reset sequence is no longer repeated in case of an error. An explicit reset command is now necessary to restart the reset sequence.
- Windows setup tool works now also with COM ports >= 10.
- Windows setup tool accepts the config file name as command line parameter.

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bdiGDB for BDI3000 MPC85xx/P10xx/P2020

Release Note

Config. program ☐ V1.05
Firmware for BDI3000 ■ V1.17

Date: Sept. 25, 2012

Enhancements

- Support for Spansion S29GL-S flash added (S29GLSX16 algorithm)
- Support for Spansion S29VS-R flash added (S29VSRX16 algorithm)
- The WREG init list entry now accepts all names from the register definition file.
- The new Telnet command UPDATE allows to reload the BDI configuration and register definition file without rebooting the BDI.
- The JTAG clock frequency can be entered in Hertz and not only as an index.
- Maximal Telnet and GDB remote command length increased to 256 characters.
- GDB: The BDI now answers with 1 to the GDB qAttached packet.
- If MMU translation is necessary, the BDI searches also TLB0 even when PTBASE is defined.
- For newer cores the BDI sets now DBCR0[FT] and executes the necessary „rfci“ instruction during a target restart. This stops now the timers while in debug halt mode.

Error Correction

- A too long GDB remote command (monitor command) no longer crashes the BDI.

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bdiGDB for BDI3000 MPC85xx/P10xx/P2020

Release Note

Config. program ☐ V1.05
Firmware for BDI3000 ■ V1.18

Date: January 21, 2014

Enhancements

- For flash algorithm MIRRORX16 and S29GLSX16 the Telnet unlock command erases the PPB bits.
- The sector erase function for S29GLSX16 uses the S29GL-S Blank Check command to test if a sector is already erased. The erase command is only execute if the sector is not already blank.
- The new init list entry WTLB allows to write L2CAM/L2TLB entries directly without the use of any helper code. A SIZE of 0 selects L2TLB (TLB0).
- Optimized Telnet commands "halt 0 1" and "go 0 1". The delay time between the start and stop of the two cores has been minimized.
- A new configuration option allows to select SMP mode, "STARTUP mode [mode [SMP]]". In this mode the BDI halts also the other core when one core halts because of a breakpoint.
- In SMP mode a "continue" command from GDB is handled different. If only one core (either core#0 or core#1) is connected to a GDB session then a "continue" command from GDB always starts both cores. If both cores are connected to GDB sessions then the first "continue" from either GDB prepares the attached core for restart but the final step to actually restart is made pending. Then a"continue" command from the GDB session assigned to the other core prepares also this core for restart and finally both cores are restarted with a minimal delay.
- The new Telnet command "state" displays the current state of all cores.
- The new startup mode WAIT allows to halt the second core at its reset vector once it has been enables by code running on the first core.
  STARTUP HALT WAIT ;halt core#0 at boot vector, halt core#1 once enabled.
- Support for little endian added. This is a gerneral switch and mixed endian is not supported. Care must be taken when accessing CCSR registers. These memory mapped registers are big endian. Have a look at regP1020LE.def. Out of reset boot space is big endian. Consider this when executing helper code. LE support was tested on a P1020RDB with the configuration p1020rdb_le.cfg. Before connecting with GDB make sure it assumes little endian and e500 architecture.

bdiGDB for BDI3000 MPC85xx/P10xx/P2020

Release Note

Config. program ■ V1.06
Firmware for BDI3000 ■ V1.19

Date: October 2, 2014

Enhancements

- Configuration and register definitions can be stored in the BDI internal Flash memory. In this case no TFTP server is necessary to load the configuration files.
- Improved software breakpoint handling in SMP mode.
- New Telnet QUERY command to display parts of the configuration.

QUERY [<core>]

Examples:

BDI> query	displays common and core specific configuration for all cores
BDI> query 1	displays the core specific configuration of the selected core

Error Correction

- Some error correction in little endian mode.

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